In the Claims

1. (Currently Amended) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate;

wherein the control gate is separated from the floating gate by a low tunnel barrier ~~integrate~~ intergate insulator having a thickness of less than 20 Angstroms;

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator.

2. (Previously Presented) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of nickel oxide (NiO), and aluminum oxide (Al_2O_3).

3. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

4. (Original) The floating gate transistor of claim 3, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, and Gd_2O_3.

5. (Original) The floating gate transistor of claim 1, wherein the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

6. (Original) The floating gate transistor of claim 5, wherein the Perovskite oxide tunnel barrier is selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

7-8. (Canceled)

9. (Original) The floating gate transistor of claim 1, wherein the floating gate transistor includes an n-channel type floating gate transistor.

10. (Currently Amended) A vertical memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate;

wherein the control gate is separated from the floating gate by a low tunnel barrier ~~integrate~~ <u>intergate</u> insulator having a thickness of less than 20 Angstroms;

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ <u>intergate</u> insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ <u>intergate</u> insulator.

11. (Previously Presented) The vertical memory cell of claim 10, wherein the low tunnel barrier intergate insulator includes an insulator selected from the group consisting of NiO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, $Gd_2\ O_3$, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

12-13. (Canceled)

14. (Previously Presented) The vertical memory cell of claim 10, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

15. (Previously Presented) The vertical memory cell of claim 14, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

16. (Previously Presented) The vertical memory cell of claim 10, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

17. (Previously Presented) The vertical memory cell of claim 16, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

18. (Original) A DEAPROM memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer, wherein the metal oxide intergate insulator has a tunnel barrier of less than 1.5 eV;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

19. (Original) The DEAPROM memory cell of claim 18, wherein first and the second metal layers are platinum (Pt) and the metal oxide intergate insulator is selected from the group consisting of TiO_2, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

20. (Original) The DEAPROM memory cell of claim 18, wherein the first and second metal layer are aluminum and the metal oxide intergate insulator is selected from the group consisting of Ta_2O_5, ZrO_2, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

21. (Original) The DEAPROM memory cell of claim 18, wherein the metal oxide intergate insulator has a thickness of less than 20 Angstroms, and wherein the metal oxide intergate insulator is selected from the group consisting of NiO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, Gd_2O_3, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

22. (Original) The DEAPROM memory cell of claim 18, wherein the first and the second metal layers are selected from the group consisting of platinum (Pt) and aluminum (Al), and wherein the metal oxide intergate insulator is selected from the group consisting of transition metal oxides and Perovskite oxides.

23. (Original) The DEAPROM memory cell of claim 18, wherein the DEAPROM memory cell includes a vertical DEAPROM memory cell.

24. (Currently Amended) A method of forming a floating gate transistor, comprising:

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a floating gate opposing the channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier integrate insulator to separate the control gate from the floating gate, wherein forming the low tunnel barrier ~~integrate~~ intergate insulator includes a tunnel barrier of less than 1.5 eV;

wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator; and

wherein forming the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator.

25. (Original) The method of claim 24, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of NiO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, Gd_2O_3, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

26. (Original) The method of claim 24, wherein forming the low tunnel barrier intergate insulator includes forming a low tunnel barrier intergate insulator having a thickness of less than 20 Angstroms.

27. (Previously Presented) The method of claim 24, wherein forming the floating gate includes the metal layer being selected from the group consisting of platinum (Pt) and aluminum (Al).

28. (Previously Presented) The method of claim 24, wherein forming the control gate includes the metal layer being selected from the group consisting of platinum (Pt) and aluminum (Al).

29. (Currently Amended) A method for operating a DEAPROM memory cell, comprising:

writing to a floating gate of the DEAPROM memory cell using channel hot electron injection, wherein the DEAPROM memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier ~~integrate~~ intergate insulator having a tunnel barrier of less than 1.5 eV,

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator, and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator; and

erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate by applying an electric field across the ~~integrate~~ intergate insulator of 2.5×10^6 V/cm.

30. (Original) The method of claim 29, wherein writing to a floating gate of the DEAPROM memory cell includes storing a charge of 1.6×10^{-6} coulombs/cm^2 on the floating gate.

31. (Original) The method of claim 30, wherein the method further includes refreshing a stored charge on the floating gate at 1.0 second intervals.

32. (Original) The method of claim 29, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate further includes:

providing a negative voltage to the substrate; and

providing a large positive voltage to the control gate such that an erase current of 1 Amp/cm^2 is created between the floating gate and the control gate, and wherein an erase of charge from the floating gate is achieved in less than 1.0 microseconds.

33. (Original) The method of claim 29, wherein the method further includes writing to the floating gate by tunneling electrons from the control gate to the floating gate.

34. (Original) The method of claim 33, wherein writing to the floating gate by tunneling electrons from the control gate to the floating gate further includes:

applying a positive voltage to the substrate; and

applying a large negative voltage to the control gate.

35. (Currently Amended) A method for operating an array of DEAPROM memory cells, comprising:

writing to one or more floating gates for a number of DEAPROM memory cells in the array of DEAPROM memory cells by tunneling electrons from a control gate through a low tunnel barrier ~~integrate~~ <u>intergate</u> insulator having a tunnel barrier of less than 1.5 eV to a floating gate, wherein the array of DEAPROM memory cells includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried source lines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of DEAPROM memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier ~~integrate~~ intergate insulator;

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of DEAPROM cells

wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator; and

wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier ~~integrate~~ intergate insulator; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates through the low tunnel barrier ~~integrate~~ intergate insulator.

36. (Original) The method of claim 35, wherein tunneling electrons through a low barrier intergate insulator includes tunneling electrons between one or more floating gates and control gates in the array through an intergate insulator selected from the group consisting of NiO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, Y_2O_3, Gd_2O_3, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

37. (Original) The method of claim 35, wherein tunneling electrons through a low barrier intergate insulator includes tunneling electrons between a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator and a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator, wherein the metal layers are selected from the group consisting of platinum (Pt) and aluminum (Al).

38. (Original) The method of claim 35, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gates further includes:

providing a negative voltage to a substrate of one or more DEAPROM memory cells; and

providing a large positive voltage to the control gate for the one or more DEAPROM memory cells.

39. (Original) The method of claim 38, wherein the method further includes erasing an entire row of DEAPROM memory cells by providing a negative voltage to all of the substrates along an entire row of DEAPROM memory cells and providing a large positive voltage to all of the control gates along the entire row of DEAPROM memory cells.

40. (Original) The method of claim 38, wherein the method further includes erasing an entire block of DEAPROM memory cells by providing a negative voltage to all of the substrates along multiple rows of DEAPROM memory cells and providing a large positive voltage to all of the control gates along the multiple rows of DEAPROM memory cells.

41. (Previously Presented) The vertical memory cell of claim 10, wherein the control gate has a tunnel barrier of less than 1.5 eV.

42. (Previously Presented) The vertical memory cell of claim 10, wherein the control gate is adapted for a Dynamic Electrically Alterable Programmable Read Only Memory.